X20DI2377

1 General Information

The module is equipped with two inputs for 3-wire connections. Both inputs can be configured as event counters. Gate measurement is only ever possible on one channel.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital inputs
- Sink connection
- 3-wire connections
- 2 counter inputs with 50 kHz counter frequency
- Gate measurement
- 24 VDC and GND for sensor supply
- Software input filter can be configured for entire module

2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI2377	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 2 event counters 50 kHz, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20DI2377 - Order data

3 Technical data

Model number	X20DI2377
Short description	
I/O module	2 digital inputs 24 VDC for 3-wire connections, special functions
General information	
B&R ID code	0x1B8E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.15 W
Internal I/O	0.82 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
EAC	Yes
KC	Yes
Digital inputs	
Nominal voltage	24 VDC
Input characteristics per EN 61131-2	Type 1
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 10.5 mA
Input circuit	Sink
Input filter	
Hardware	≤10 µs
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	3-wire connections
Input resistance	Typ. 2.23 kΩ
Additional functions	50 kHz event counting, gate measurement
Switching threshold	
Low	<5 VDC
High	>15 VDC
Insulation voltage between channel and bus	500 V_{eff}
Event counters	
Quantity	2
Signal form	Square wave pulse
Evaluation	Every rising edge, cyclic counter
Input frequency	Max. 50 kHz
Counter 1	Input 1
Counter 2	Input 2
Counter frequency	Max. 50 kHz
Counter size	16-bit
Gate measurement	
Number of gate measurements	1
Signal form	Square wave pulse
Evaluation	Rising edge - falling edge
Counter frequency	
Internal	48 MHz, 24 MHz, 12 MHz, 6 MHz, 3 MHz, 1.5 MHz, 750 kHz, 375 kHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 1 or Input 2
Sensor power supply	
Power consumption	Max. 12 W [1)]
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short-circuit protection at 500 mA	Max. 2 VDC

Table 2: X20DI2377 - Technical data

Model number	X20DI2377
Summation current	0.5 A
Short-circuit proof	Yes
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Pitch	$12.5^{+0.2}$ mm

Table 2: X20DI2377 - Technical data

1) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

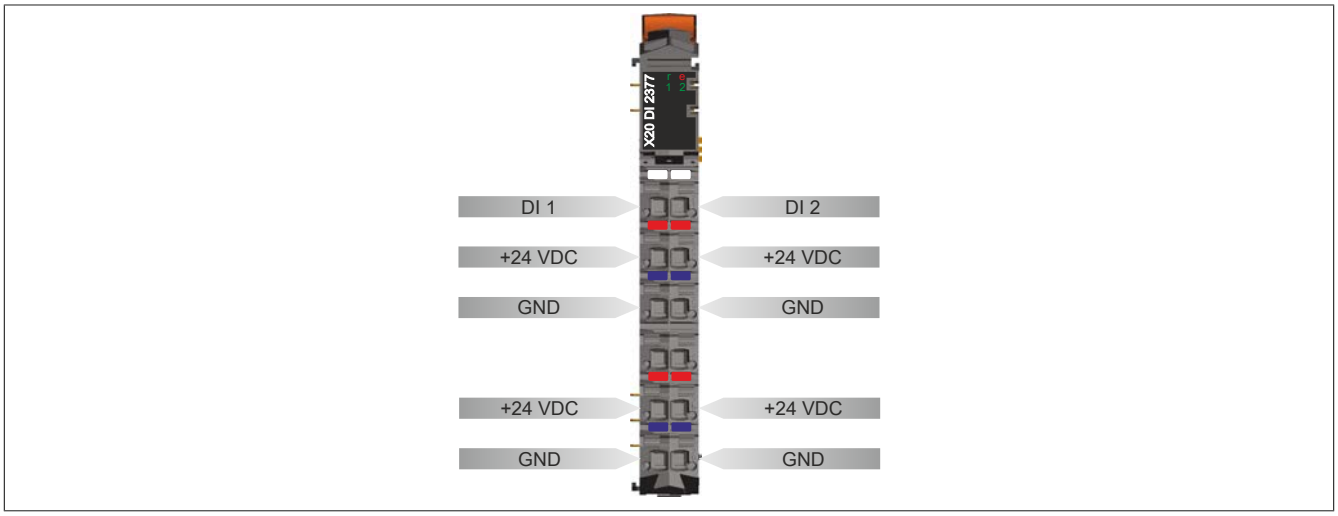
4 Status LEDs

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

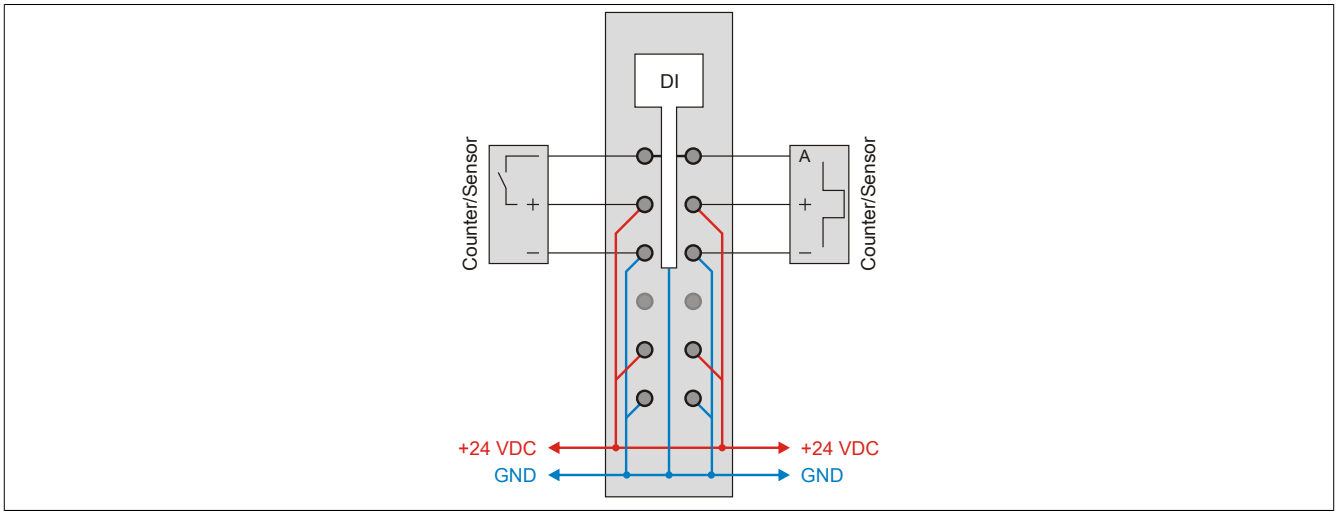
Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green		Input status of the corresponding digital input

5 Pinout

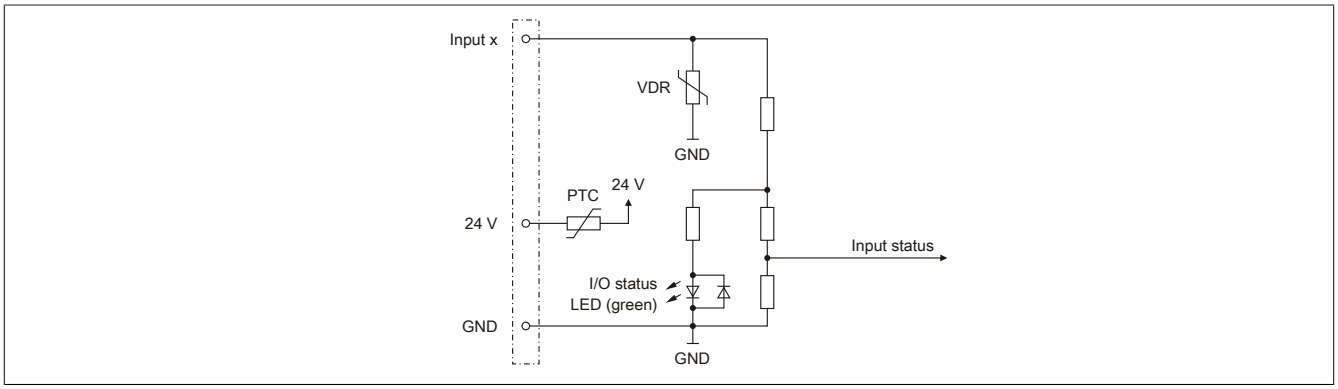
Auxiliary contacts are provided on the module for easy wiring. VDC and GND contacts are internally connected and can be loaded with a total of 0.5 A (see section "Connection example" on page 4).



6 Connection example

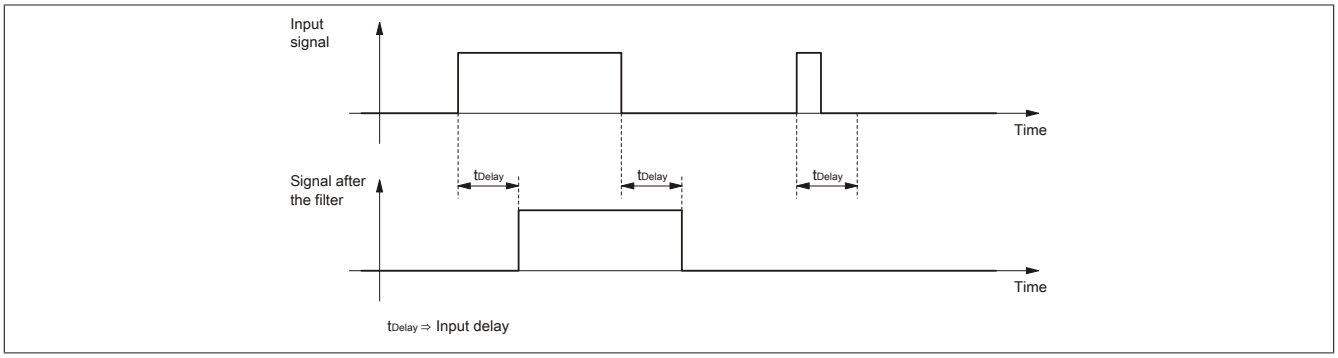


7 Input circuit diagram



8 Input filter

An input filter is available for each input. The input delay can be set using register "ConfigOutput01" on page 7. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



Information:

The input filter is applied to digital inputs in event counter mode with software

The input filter is NOT applied in event counter mode without software.

9 Register description

9.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
18	ConfigOutput01 (input filter)	USINT				•
20	ConfigOutput02 (configuration counter 1)	USINT				•
22	ConfigOutput03 (configuration counter 2)	USINT				•
Communication						
0	DigitalInput	USINT	•			
	DigitalInput01	Bit 0				
	DigitalInput02	Bit 1				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Counter configuration	USINT			•	
	ResetCounter01	Bit 5				
22	Counter configuration	USINT			•	
	ResetCounter02	Bit 5				

9.3 Function model 1 - Input latch

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
18	ConfigOutput01 (input filter)	USINT				•
20	ConfigOutput02 (configuration counter 1)	USINT				•
22	ConfigOutput03 (configuration counter 2)	USINT				•
Communication						
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Counter configuration	USINT			•	
	ResetCounter01	Bit 5				
22	Counter configuration	USINT			•	
	ResetCounter02	Bit 5				
26	Input status of digital latch inputs 1 - 2	USINT	•			
	DigitalInputLatch01	Bit 0				
	DigitalInputLatch02	Bit 1				
28	Acknowledge digital inputs	USINT			•	
	DigitalInput01LatchQuitt	Bit 0				
	DigitalInput02LatchQuitt	Bit 1				

9.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
18	-	ConfigOutput01 (input filter)	USINT				•
20	-	ConfigOutput02 (configuration counter 1)	USINT				•
22	-	ConfigOutput03 (configuration counter 2)	USINT				•
Communication							
4	0	Counter01	UINT	•			
6	2	Counter02	UINT	•			
20	-	Counter configuration	USINT				•
		ResetCounter01	Bit 5				
22	-	Counter configuration	USINT				•
		ResetCounter02	Bit 5				

1) The offset specifies where the register is within the CAN object.

9.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

9.4.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

9.5 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

9.5.1 Digital input filter

Name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter (bus controller default setting)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

9.5.2 Input status of digital inputs 1 to 2

Name:
DigitalInput or
DigitalInput01 to DigitalInput02

The input status of digital inputs 1 to 2 is mapped in this register.

Only function model 0 - Standard:

The "packed inputs" setting in the Automation Studio I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the Automation Studio I/O mapping ("DigitalInput01" through "DigitalInput02") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 3	Packed inputs = On
	See the bit structure.	Packed inputs = Off or function model ≠ 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
1	DigitalInput02	0 or 1	Input state - Digital input 2

9.5.3 Input status of digital latch inputs 1 - 2

Name:
DigitalInputLatch01 to DigitalInputLatch02

The input status of digital inputs 1 to 2 after expiration of the input filter time is mapped in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInputLatch01	0 or 1	Input status of digital input 1 after expiration of the delay time
1	DigitalInputLatch02	0 or 1	Input status of digital input 2 after expiration of the delay time

9.6 Counter operation

The following operation modes can be selected:

- Event counter mode
- Event counter mode with software (processed after the input filter)
- Gate measurement

Event counter mode

The rising (positive) edges are registered on the counter input.

The counter state is registered with a fixed offset with respect to the network cycle and transferred in the same cycle.

Event counter mode with software

The rising (positive) edges are registered on the counter input. But the edges are first processed through the configured software filter.

The counter state is registered with a fixed offset with respect to the network cycle and transferred in the same cycle.

Gate measurement

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF) and corrected with the adjustable prescaler.

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

> **Information:**
>
> **Only one of the counter channels at a time can be used for gate measurement.**

9.6.1 Event or gate counter

Name:
Counter01 to Counter02

This register displays the results of the individual counters.

Event counter or gate measurement (16-bit counter value) depending on operating mode.

- **Configuration as an event counter**
  This register contains the counter value of all positive edges on the input channel.
- **Configuration as gate measurement**
  This register contains the counter value between positive and negative edges on the input channel. The absolute time duration depends on the set frequency.

Data type	Value	Information
UINT	Counter value	Default value = 0

Calculating the gate measurement

The measuring frequency can be set between 48 Mhz and 375 kHz (see "Counter configuration " on page 9). The maximum time to be measured depends on the height of the measuring frequency. The higher the measuring frequency, the shorter the measurable time period.

Formula for converting the counter value into time

$$Time_{ms} = \text{Counter value} * \frac{1}{\text{Measuring frequency}_{Hz}}$$

Examples

3485 * (1 / 375000 Hz) = 9.2933 ms

10345 * (1 / 750000 Hz) = 13.7933 ms

33719 * (1 / 187500 Hz) = 179.834 ms

55760 * (1 / 6000000 Hz) = 9.2933 ms

9.6.2 Counter configuration

Name:
ConfigOutput02 to ConfigOutput03

This register can be used to configure the individual counters.

Data type	Value	Bus controller default setting
USINT	See bit structure.	0

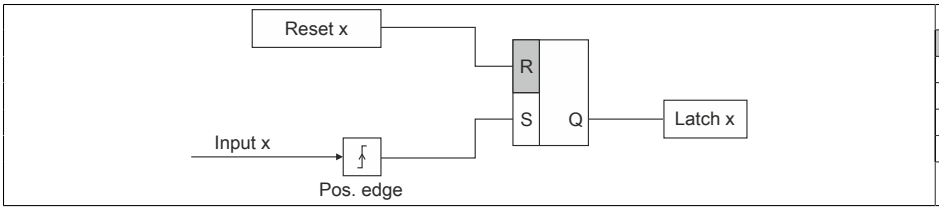
Bit structure:

Bit	Name	Value	Information
0 - 3	Counter frequency	0	48 MHz (only for gate measurement) (bus controller default setting)
		1	3 MHz (only with gate measurement)
		1	**Event counter** via software (only in event counter operation)
		2	187.5 kHz (only with gate measurement)
		3	24 MHz (only with gate measurement)
		4	12 MHz (only with gate measurement)
		5	6 MHz (only with gate measurement)
		6	1.5 MHz (only with gate measurement)
		7	750 kHz (only with gate measurement)
		8	375 kHz (only with gate measurement)
4	Reserved	0	
5	ResetCounter01 or ResetCounter02	0	No influence on the counter
		1	Clear counter (at rising edge)
6 - 7		0	Event counter measurement (bus controller default setting)
		1	Gate measurement

9.7 Rising edge input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

9.7.1 Acknowledge digital inputs

Name:
DigitalInput01LatchQuitt to DigitalInput02LatchQuitt

This register is used to reset the input latches channel by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
1	DigitalInput02LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
2 - 7	Reserved	-	

9.8 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

9.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs